formed by implantation through a single mask formed on the SOI substrate.

20. The method of claim 18, further comprising:

forming a mask having openings on the SOI substrate;

depositing an emitter material contacting the SOI substrate having a first impurity in said openings in a damacene process to form emitters; and

annealing the SOI substrate to drive said first impurity into said base region to create an emitter diffusion region in said base region below each emitter.

Remarks

Applicants respectfully request that this amendment be entered, and that their subject U.S. Patent application be passed to issuance in view thereof. The foregoing amendments are further indicated in blackline form in Exhibit A, "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Applicants have amended the Specification to correct the error noted by the Examiner. Applicants have also amended claims 5, 10, and 16 to address the §112 rejections thereto.

In the Office Action, pending claims 1-4, 6-9, 11-15, and 17 stand rejected under 35 U.S.C. 103 in view of various combinations of the teachings of U.S. Patent 5,406,113 ("Horie"), U.S. Patent 6,037,664 ("Zhao"), and 6,284,581B1 ("Pan"). In response, Applicants respectfully submit that these various combinations of references neither teach nor suggest the invention as recited in the claims as presented herein.

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In the invention, a damascene process is utilized to form an emitter that is used as a diffusion source for a dopant region that is subsequently formed in the base region underlaying the emitter. The damascene emitter reduces junction capacitances and enhaces bipolar-CMOS integration. The self-aligned diffusion from the damacene emitter reduces critical masking requirements and decreases cell size.

More particularly, with reference to Fig. 5 of the invention, note that while there is gate oxide 32 between the gate electrode 30 and the substrate 12 in the CMOS regions, there is no gate oxide between the emitters 42 and the substrate 16. While as a practical matter dopant can outdiffuse through a gate dielectric, such a structure is not preferable because the drive-in energy of the anneal to produce the outdiffusion will have to increase, either by time or by temperature, over the anneal required without the gate dielectric. Such higher drive-in energies are to be avoided in current process designs.

As to the prior art of record, note that (as correctly indicated by the Examiner) Horie does not teach or suggest forming a damascene emitter, as set forth in the present claims. In the Office Action the Examiner states that Zhao would suggest a damascene emitter. Applicants respectfully disagree. Note that Zhao teaches that the damascene material 10 is either copper or aluminum, and that the damascene material is separated from the substrate by a "barrier" (in the case of copper, to prevent copper diffusion) or a "liner" (in the case of aluminum, to promote adhesion). See Col. 5, lines 1-38. As such, Zhao teaches that the damascene material is always separated from the substrate by a barrier or liner material. In the invention, the emitter contacts the substrate, such that a diffused region is subsequently formed by outdiffusion. Zhao neither teaches nor suggests such a process. One of the purposes of a banner or liner material is to prevent material interactions between the damascene material and the underlaying substrate; in other words, such layers are intended to prevent the types of interactions inherent in an out diffusion process. Moreover, note that neither copper nor aluminum are doped with conductivity-altering dopants to form a region by outdiffusion. In fact, such metals are normally

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not used as sources of dopant because they typically cannot withstand the high annealing temperatures required for outdiffusion, whether or not a barrier or liner layer is present. Thus, Applicants respectfully submit that if anything, Zhao teaches away from, rather than toward, a damascene emitter.

Applicants respectfully submit that the aforementioned shortcomings in the teachings of Zhao are not provided by the Pan reference, because Pan does not depict a damascene process.

Thus, Applicants respectfully submit that their invention is patentable over the Horie, Zhao, and Pan references applied in the Office Action, in that Zhao teaches away, rather than toward, the suggested combination. Both Zhao and Pan teach that the conductor in question is separated from the substrate by an intervening material. Zhao teaches a damascene conductor - and in that teaching, the conductor is separated from the substrate by an intervening material. Applicants respectfully submit that the Examiner cannot combine the teachings of the Horie and Zhao references while omitting the intervening barrier/liner layer which is taught by Zhao as being necessary for the Zhao invention (note e.g. all of independent claims 1, 11, and 26 of Zhao specify the presence of a barrier layer), because to do so would constitute the use of hindsight reconstruciton. Put another way, removing the barrier layer of Zhao would render it inoperable for its intended purpose; as such Zhao leads away from such an obviousness combination.

Applicants have amended claims 1 and 12 to make it clear that the emitter material contacts the substrate. Applicants have rewritten claim 11 into independent form, and such claim has been further amended to specify that a gate oxide is only formed where the CMOS gates are to be formed (and not in the emitter regions - note that in Pan the gate ox is formed in both the bipolar and CMOS regions).

Finally, Applicants have added new claims 18-20. Claim 18 is in independent form, and recites the collector disposition and collector-base stacking features of the invention as discussed at page

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6, line 17 through page 7, line 11 and as shown in Fig. 1 (as well as virtually all of the remaining Figures). The significance of these features of the invention in reducing base width while reducing collector capacitance is discussed at page 7, lines 12-16. Applicants respectfully submit that the recited collector structure and collector-base stacking is neither shown nor suggested by any reference of record, alone or in combination. Claim 19 (dependent on claim 18) specifies that the two regions are formed through a single mask, as taught at page 7, lines 17-18. Claim 20 (also dependent on claim 18) recites a damascene emitter that contacts the substrate and serves as an outdiffusion source, as discussed above. Applicants respectfully submit that these new claims 18-20 recite patentable aspects of the invention in view of the references of record.

Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments, questions, or suggestions, please do not hesitate to contact the undersigned attorney at the telephone number and/or email address set forth below.

Respectfully submitted,

For: Divakaruni et al.

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Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Delete the paragraph starting on line 5, page 7, and replace it with the following:

In one preferred embodiment, the SOI layer 10, 12 15 could have a thickness of approximately 400nm. The collector 14 implant 19 preferably has a dose of $1x10^{16}cm^{-2}$ [$1x1016cm^{-2}$] at a power of 1M3V. This doping profile (and other similar doping profiles that would be known by those ordinarily skilled in the art given this disclosure) produces a buried collector 14 centered at approximately the back interface of the silicon 15 and insulator or 12 layers with a peak concentration of approximately $3x10^{19}cm^{-3}$.

In the Claims:

1. (Amended) A method of forming an emitter in a vertical bipolar transistor comprising:
providing a substrate having a collector layer and a base layer over said collector layer;
forming a patterned mask over said base [collector] layer; and
filling openings in said mask with emitter material in a damascene process, said emitter material contacting the substrate.

5. (Amended) The method in claim 2, further comprising:
forming a protective layer over said emitters; and
implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

Cancel claim 6.

7. (Amended) The method in claim [6] 11, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:
implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and
implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

10. (Amended) The method in claim 7, further comprising:

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forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

11. (Amended) [The method in claim 6 further comprising, before said forming of said polysilicon,] A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

forming a gate oxide layer over only said CMOS region of said SOI substrate;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

12. (Amended) A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

13. (Amended) The method in claim [12] 14, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

14. (Amended) [The method in claim 13] A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated

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circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters, said emitters contacting said SOI substrate;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

16. (Amended) The method in claim 13, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into and through said insulator layer to provide a collector contact diffusion region.

17. (Amended) The method in claim 14 [12], further comprising, before said forming of said polysilicon, forming a gate oxide layer over only said CMOS region of said SOI substrate.

Please add the following new claims:

18. A method of forming a bipolar device on a SOI substrate having a buried insulator layer that forms an interface with an overlying semiconductor layer, comprising the steps of:

forming in said semiconductor layer a buried collector region contered at approximately said interface; and

forming in said semiconductor layer a base region vertically stacked on said buried collector region.

19. The method of claim 18, wherein said buried collector region and said base region are formed by implantation through a single mask formed on the SOI substrate.

20. The method of claim 18, further comprising:

forming a mask having openings on the SOI substrate;

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depositing an emitter material contacting the SOI substrate having a first impurity in said openings in a damacene process to form emitters; and

annealing the SOI substrate to drive said first impurity into said base region to create an emitter diffusion region in said base region below each emitter.

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